Hailiang Hu

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Objective

- PhD student looking for **fulltime** in **EDA**, **Software Engineer**

Technical Skills

Programming Languages: C++, Python, Tcl Script, Linux/Shell
Hardware: FPGA, VLSI, Synthesis, Placement, Physical Design

Education

Ph.D. in Electrical & Computer Eng, Texas A&M University (GPA:3.78/4.0) Sep 2019 - Dec 2025

M.S. in Electrical Eng, Northwestern University (GPA:3.74/4.0) Aug 2015 - Dec 2016

B.A in Electrical Eng, Harbin Institute of Technology, China (GPA:3.78/4.0) Aug 2011 - Jul 2015

Core Courses: Analysis of Algorithms, Data Structure, VLSI Design Automation, Machine Learning

Academic Experience

Graduate Research Assistant, Texas A&M University Jun 2020 - Present

Hardware Acceleration of Machine Learning Models

- Analyzed the performance, and hardware cost of machine learning models on FPGAs
- Proposed algorithms for performance improvement and high-efficiency implementation

Systolic Array Placement on FPGA

- Developed a macro placement algorithm for CNN circuits on FPGAs
- Improved wirelength by 24% compared with state-of-the-art placement tools
- Achieved empirical optimal solution on the 2D macro array placement with constant runtime

FPGA Macro-Placement Contest

- Achieved the fourth-place awards in the MLCAD Contest (2023)
- Implemented the core global placement engine with support of various constraints on modern FPGAs

Wafer-Scale Physics Modeling Contest

- Achieved the first-place awards in the International Symposium on Physical Design Contest (2021)
- Collaboratively implemented a placement tool that maps the finite element computing units onto the Wafer-scale engine
- Reduced the wire length by 6% by implementing the detailed placement algorithms

Graduate Teaching Assistant, Texas A&M University Jan 21 - Present

Machine Learning for Electrical Engineers

- Facilitated students with lab assignments on machine learning for practical engineering use-cases
- Coached student groups on final projects, including dataset management, ML model development, and deployment

FPGA Information Processing Systems

- Designed the lab manuals and materials to facilitate students working on lab assignments
- Guide students on the implementation of signal processing and neural network applications on FPGAs with Verilog
- Led weekly lab sessions in groups of 50 students

Professional Experience

Student Researcher, Google DeepMind - Mountain View, CA May 2024 – Aug 2024

- Worked on VLSI optimization for circuit performance improvement
- Implemented algorithms for circuit analysis and critical path identification
- Implemented performance-driven placement techniques and reduced critical path wirelength over 10%

Software Development Intern, AMD (Xilinx) - San Jose, CA May 2023 – Aug 2023

- Worked on placement techniques for wirelength improvement
- Developed a machine learning model for routed wirelength estimation to guide placement
- Implemented deep-learning toolkit accelerated placement techniques for routing-aware placement

Software Development Intern, AMD (Xilinx) - San Jose, CA May 2022 – Aug 2022

- Developed and integrated a machine learning-based circuit delay prediction framework in the commercial tool
- Improved the accuracy of delay estimation by 56x compared with the existing heuristic method
- Saved 87.5% on runtime compared with the technology mapper

Embedded Engineer, Suzhou Collaborative Medical Robot Institute - Suzhou, China Apr 2017 – Jun 2019

Exoskeleton Rehabilitation Robotics

- Developed the embedded software of rehabilitation robots based on Beckhoff PLC
- Implemented the communication protocol in the embedded system for sensor and motor control
- Coordinated with mechanical engineers on designing and building the hardware platform

Publications

[C4] **H. Hu**, D. Fang, W. Li, B. Yuan, J. Hu. Systolic Array Placement on FPGAs. International Conference on Computer-Aided Design (**ICCAD**), 2023

[C3] **H. Hu**, J. Hu, F. Zhang, B. Tian, and I. Bustany. Machine-Learning Based Delay Prediction for FPGA Technology Mapping. System Level Interconnect Pathfinding (**SLIP**), 2022

[C2] D. Fang, B. Zhang, **H. Hu**, W. Li, B. Yuan, and J. Hu. Global Placement Exploiting Soft 2D Regularity. International Symposium on Physical Design (**ISPD**), 2022

[C1] Y. Lin, R. Liang, Y. Li, **H. Hu**, J. Hu. Mapping Large Scale Finite Element Computing on to Wafer-Scale Engines. Asia and South Pacific Design Automation Conference (**ASP-DAC**), 2022